Digital Circuit Design

Course Code: BBU5202 Electronic Engineering Department

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| Lab Sheet 3: Introduction to Design using VHDL | Date: **\_\_2015/6/8\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_** |
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1. **Learning Objectives**

The aims of this Lab Session is to learn how to use VHDL and ModelSim to design and simulate some basic logic circuits, namely: a NAND gate.

1. **VHDL Experiment steps**

The first stage in the design of my circuit is to create one of the most basic components; this is the NAND gate.

**2.1.1. Creating a Project**

>> Open the Xilinx Project Navigator tool.

>> Create a directory where I save my project.

>> (Xilinx Project Navigator) Select the option **File → New Project…**

>> After filling in the appropriate fields, click the **Next >** button.

>>Choose the settings **Spanrtan2**.

>>Click the **Next >** button.

I now have a project that will contain all your designs, test benches and results. In addition, I can see a window entitled “New Project”, containing an empty table with the fields: **Source File** and **Type**.

The first step in creating a VHDL design is to create the Entity and Architecture pair. In order to do this, I add a new source to my project.

>> Click the **New Source…** button. A window, named “New Source” should appear.

>> Give an appropriate name to the entity, under the tab **File Name**.

>> Ensure I have selected these options in the same window: **VHDL Module** and **Add to project**.

>>Click the **Next >** button in this window and the following one. I can now see a window with a summary of my source.

>> Click the **Finish** button and I can see a window entitled “New Project”.

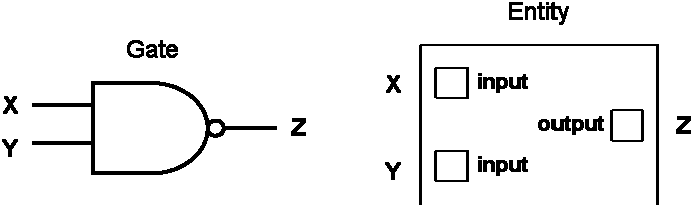
>> Click the **Next >** button in this window and the following one. This results gives a summary of the project created. Once the project is created, I can proceed to add a new source to your project.

>> Click the **Finish** button.

I can now see a window displaying on the right hand side of my main ISE Project Navigator window, after clicking on the button labelled ***sourceName*.vhd**.

**2.1.2. Creating the Entity**

The Entity declaration describes the device’s interface. This means describing the ‘ports’ and their directions. The NAND gate I will design can be described as below (see **Figure 1**). **Note**: Assume that each input and output is *1-bit* long.



**Figure 1** – NAND Gate and Entity: representation.

The VHDL code that describes the entity indicated in **Figure 1**, is as below. Copy the code to the VHDL tool window and save the file.

Entity NAND1 is

Port (X, Y: in std\_logic;

Z: out std\_logic);

End NAND1;

**2.1.3. Creating the Architecture**

Next, I need to describe our architecture. The architecture describes the entity’s functionality. Copy the code to my VHDL tool window and save the file.

Architecture Behavioral of NAND1 is

begin

Z <= X nand Y;

end Behavioral;

**2.1.4. Creating the Test Bench**

To run the simulation of my design, I use the ModelSim simulator which requires two kinds of inputs: the circuit description VHDL source file, and a set of stimulus values that define all inputs’ logic and duration.

My steps:

>> Select the ***sourceName*.vhd** tag in the “Project” window.

>> Select the **Project→New Source…** option.

>>Select the **Test Bench Waveform** option. >>Name the file as “*sourceName\_*tbw”.

>>Click the **Next >** button. Ensure that the next window has my chosen “*sourceName*” selected as the associated source.

>>Click the **Next >** button again.

A new window called “New Source Information” appear, containing the test bench specification for the source we chose.

>>Click the **Finish** button.

The HDL Bencher is launched and will be ready for the timing parameters to be entered

>> Change the “Clock Information” to use the option **Combinatorial (or internal clock)**.

>> Click the **OK** button.

>>manipulate the input waveforms.

>> Save the testbench (**File→Save (the waveform)**) and shut it down.

**2.1.5. Generating the Simulation Output Values**

>> In the “Sources in Project” window, select the ***sourceName*\_tbw (*sourceName*\_tbw.tbw)** option.

>> In the “Processes for Source: *sourceName*\_tbw” window, I see the ModelSim Simulator listed as a process. Double-click the **Simulate Behavioral Model** option (on the lefthand side).

The ModelSim simulator opened and run my simulation to the end of the test bench.

>> Exit the ModelSim tool.

1. **Experiment Conclusion**

To achieve a circuit in VHDL, we need to create an object, create an entity, create the architecture, and create the test bench and the simulation output values.